THE IMPACT OF CHANNEL DOPING DENSITY ON NANO-SCALED MOS DEVICES

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Abstract

As Metal Oxide Semiconductor (MOS) channel length shrinks into the nano-scale regime, the impact of channel doping density has become more pronounced on transistor drive current, the threshold voltage and the leakage current. This work focused on understanding the impact of channel doping density on nano-scale metal oxide semiconductor devices. Two channel doping concentrations of $5x10^{16}$ atoms/cm^3 and $5x10^{14}$ atoms/cm^3 for N-type devices with 90nm and 900nm channel lengths were evaluated. The experimental results demonstrated that the threshold increases with the higher channel doping concentration, and the variation in figure-of-merit parameters (Vt, Ioff and SS) are much greater for the lower channel doping concentration devices.

Introduction

The Metal Oxide Semiconductor Field Effect Transistor (MOSFET) has been the major device for integrated circuits over the past five decades. With technology advancement and the high scalability of the device structure, silicon MOSFET-based Very Large Scale Integrated (VLSI) circuits have continually delivered performance gains and cost reduction to semiconductor microchip manufacturers of data processing and memory devices [1]. The impact of channel doping density on MOS nano-scaled devices is vital to the design and application of devices. Since the creation of the first transistor, inventors have been trying to find ways of making devices ever smaller for economy of scale. The applications for ICs have increased, their sizes have decreased and functionality has increased. Channel length is important in the determination of off-state current [2], [3]. In this study, the average off-state leakage current for the n-channel metal oxide semiconductor (NMOS) 90nm device was 10nA and 1.1nA for the 900nm device. The transistor off-state current is defined as the drain current when the gate-to-source voltage is 0V [3]. The data presented represent an average of 244 sites at room temperature.

Experimental Methodology

The MOSFETs were fabricated using 90nm process technology. Processing was performed on 200mm diameter wafers. Lightly doped drain regions were implanted along with halo implantation in order to control the short channel effects (SCE). Threshold variation was given by way of threshold voltage implants that allowed a threshold range between low channel doping concentrations (LCDC) and high channel doping concentrations (HCDC), respectively. Two n-type devices with aspect ratios of 4500nm/90nm (W/L) and 4500nm/900nm (W/L) were tested. The high channel doping (HCDC) devices had 10^{16}cm^{-3} impurity concentrations in the channel, while the lower channel doping (LCDC) devices had 10^{14}cm^{-3} impurity concentrations in the channel. The average threshold voltage for the 90nm lower doping concentration device was 0.14V, while the value virtually doubled (0.25V) for the high channel doping concentration device. The average threshold voltage for the 900nm lower channel doping concentration devices was 0.15V, with 0.21V for the high doping concentration device. All of the devices had equal widths of 4500nm.

The data for this study were collected at the Advanced Device Characterization Laboratory of Prairie View A&M University. All measurements were performed on an Agilent 4155C Semiconductor Parameter Analyzer. Static current/voltage characteristics of front channel $I_d - V_g$ were measured with medium integration time and single sweep. The gate voltage for the n-type devices was swept from −0.20V to +1.2V in 100mV increments.

Background

In contemporary integrated circuit design, sources of power dissipation in CMOS circuitry can be attributed to sub-threshold leakage currents and dynamic switching power [3]. The largest contributor to this power-consumption challenge is dynamic switching power. This is attributed to very high speed gate capacitance charge fluctuations during signal switching. However, continued advancements in low-power voltage scaling will bring about an increase in sub-threshold leakage. This increase may be large enough in magnitude to potentially dominate overall power dissipation. In addition, this becomes more important as sub-threshold leakage current is a strong function of, and exponentially impacted by, the threshold voltage [4], [5].

Threshold Voltage Adjustment

Silicon transistor technologies have been particularly attractive for low-power applications. The challenge, as mentioned, is to minimize power dissipation while maintaining high-performance operation. The primary approach for improved energy efficiency is power supply scaling. In order to preserve circuit speed, scaling of the power supply should be accompanied by a threshold voltage reduction [2], [4]. However, the lower limit of the threshold voltage is set by the amount of tolerable off-state leakage current. This consideration becomes increasingly important with added geometric scaling to deep sub-micron regimes. Also, with power supply scaling comes a relational downward scaling of threshold voltage, which therefore makes threshold voltage control progressively important [5], [6].

The main enablers of threshold voltage adjustment can be seen in the influence of the acceptor concentration in Equation 1. The threshold voltage controlling mechanism is a function of substrate doping (N_A), substrate bias via (φ_s) and oxide thickness (t_{ox}). The primary contributor to leakage current and transistor threshold voltage will be variation of the channel doping concentration:

$$V_T = 2\varphi_F - \frac{Q_S(2\varphi_F)}{C_{ox}} + V_{FB} \qquad (1)$$

where C_{ox} is the oxide capacitance, V_{FB} is the flat band voltage, Q_s is the bulk charge, V_T is the threshold voltage and φ_F is the internal potential.

The channel doping concentration can be modified using ion implantation with two limiting cases considered: the very shallow heavily doped surface layer, and the general ion-implanted impurity profile. The very shallow surface layer is modeled in Equation 2, while the effect on threshold voltage is described by Equation 3:

$$N_D(y) = N_A + D_I\delta(0) \qquad (2)$$

$$V_G = \varphi_S + \frac{q}{C_{ox}}\int_0^W [N_A + D_i\delta(0)]dy + V_{FB}$$

$$= \varphi_S + \frac{qN_AW}{C_{ox}} + \frac{qD_i}{C_{ox}} + V_{FB} \qquad (3)$$

where V_G is the gate voltage at threshold, W is the maximum depletion width, φs is the surface potential, D_I represents the change to the channel impurity, and N_D and N_A are the donor and acceptor concentrations, respectively.

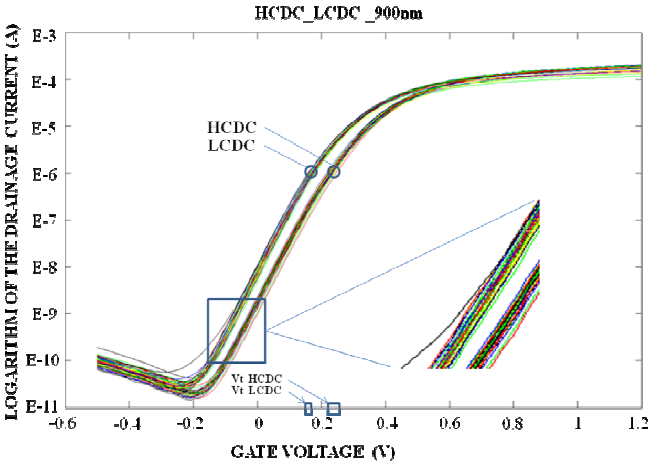

Figure 1. Current-Voltage Characteristics of HCDC and LCDC Devices of 900nm Channel Length

Results and Discussion

The data presented represent an average of 244 site measurements. As shown in Figure 1, the current-voltage characteristics of the high channel doping concentration (HCDC) and the lower channel doping concentration (LCDC) 900nm devices exhibited standard characteristics. As expected, LCDC showed higher drive current, 4.3μA for LCDC and 1.10μA for HCDC, due to less impurity in the channel. Comparatively, Figure 2 shows similar current-voltage characteristics for 90nm devices. It can be argued that both HCDC and LCDC exhibited higher variation as depicted in the figure. The average drive current of 4.3μA for LCDC and 1.10μA for HCDC remain unchanged; however, the standard deviation doubled to 6% from 2.8% for 900nm channel devices. As the voltage approached the off states, more variation was observed with the LCDC devices. This variation was attributed to larger depletion extrusion into the channel region. Although the average current was not significantly different, the variation was apparent between the 900nm (Figure 1) and 90nm (Figure 2) devices. This was expected since depletion is inversely proportional to the channel doping concentration (see Equation 4) [7], [8].

$$W_{dep} = \left[\frac{2K_s\varepsilon_0}{q}\left(\frac{N_a + N_d}{N_aN_d}\right)(V_{bi} - V)\right]^{1/2} \qquad (4)$$

Consistently apparent in Figures 1 and 2 is the higher drive current of LCDC over HCDC, both at 90nm and 900nm channel length at a given gate voltage. This is due to lower carrier mobility in HCDC channel because of the higher impurity concentration; the opposite will be the case for the LCDC devices. As shown in Figure 3, the effect of channel doping concentration on mobility is further demon-

strated. The drive currents of 90nm and 900nm channel devices are almost identical for HCDC except at higher gate voltages where 90nm drives higher. This higher drive current can be directly attributed to a higher electric field for 90nm devices and an inverse relationship between the drive current (I_D) and the channel length (see Equation 5):

$$I_D = q\frac{kT}{q}\sqrt{\frac{\varepsilon_s}{2qN_a\varphi_s}}D_n W\frac{1}{L}\frac{n_i^2}{N_a}e^{q\varphi_s/kT} \qquad (5)$$

where L is the channel length, k is the Boltzmann constant, q is the electronic charge and T represents absolute temperature. A similar argument holds for LCDC 90nm and 900nm channel length devices, as shown in Figure 4.

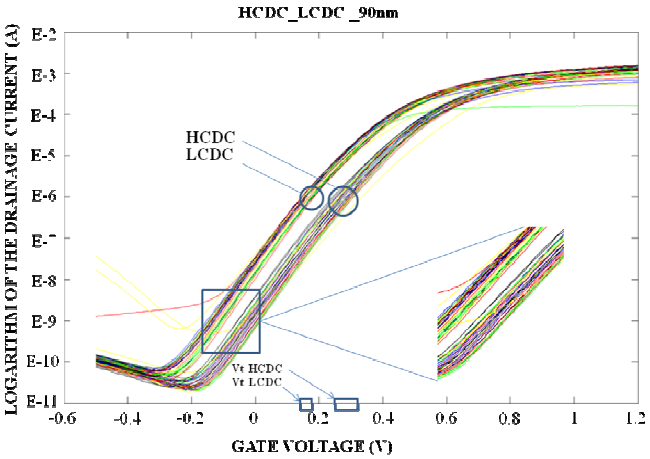

Figure 2. Current-Voltage Characteristics of HCDC and LCDC Devices at 90nm Channel Length

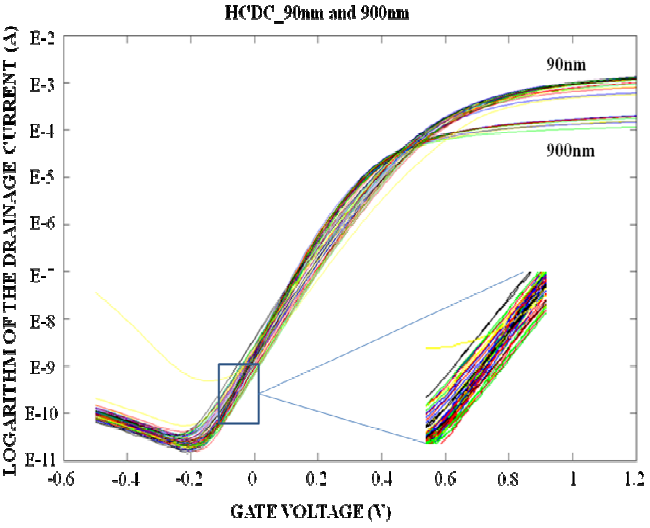

Figure 3. Current-Voltage Characteristics of 90nm HCDC and 900nm HCDC devices

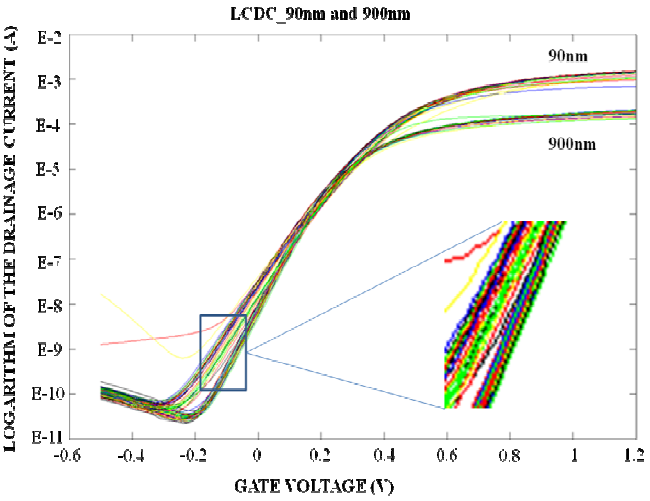

Figure 4. Current-Voltage Characteristics of 90nm LCDC and 900nm LCDC devices

It can be seen that a few sites of the 90nm devices are beginning to show higher current at very low gate voltage. This may be attributed to the higher carrier concentration in the source and drain and the associated diffusion gradient, though more drive current and more leakage current will be generated by the smaller channel devices. The sub-threshold slope for the smaller devices ranges between 96.3mV/decade and 128.6mV/decade, and between 78.2mV/decade and 102.8mV/decade for the 900nm devices.

Conclusion

Two channel length (90nm and 900nm) devices with two channel doping concentrations were characterized. At room temperature, a lower doping concentration exhibited higher leakage when compared to the high channel doping concentration device. As the channel length decreases, the I_{off} increases due to source and drain junction proximity, diffusion gradient and the higher electric field. The threshold voltage of the high channel doping concentration device is clearly much greater than the lower channel doping devices. As the channel doping concentration increases, the threshold voltage increased. The results showed that 90nm devices turn on faster with a steeper current curve. So, for a large change in Vg, there is a smaller change in the logarithm of the drain current and, consequently, a larger sub-threshold slope. In future studies, the focus will be on understanding current leakage mechanisms; specifically, gate-induced drain leakage (GIDL) and gate-edge direct tunneling and the associated quantum effects.

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