A REDUCED-CODE LINEARITY TEST FOR DAC USING WAVELET ANALYSIS

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Abstract

In selecting Digital-to-Analog converters, overall performance accuracy is a primary concern; that is, how close does the output signal reflect the input codes. Integral NonLinearity (INL) error is a critical parameter specified by manufacturers to help users determine device performance and application accuracy. In classical testing of INL error, for an n-bit DAC, 2n output levels must be included in the computation. This leads to a time-intensive and costly process. Therefore, the authors investigated the ability of Wavelet Transform to estimate INL with fewer samples in real-time testing. Compared with classical testing, the novel implementation of this Wavelet Transform has shortened testing times and reduced computational complexity based on special properties of the multi-resolution process. As such, the Discrete Wavelet Transform can be especially suitable for developing a low-cost, fast-test procedure for high-resolution DACs.

Introduction

In today's advanced communication systems, fast Digital Signal Processing (DSP) combined with mixed-signal Digital-to-Analog Converters (DACs) create a bottleneck in digital-to-analog conversion systems [1]. Therefore, it is important to determine the right DAC for the application. At the most basic level, converter testing would appear to be a simple matter. However, testing is extremely expensive and time–consuming, as many have agreed [1]-[8] for both static and dynamic parameters. Static parameters of DACs, such as Deferential Non-Linearity (DNL) and Integral Non-Linearity (INL) errors, provide specific information that show the device output monotocity and signal distortions. INL measurements, then, can be one of the major error characteristics of defining the overall DAC worst-case deviation [9]. This measurement can be lengthy and complicated, especially with the exponential growth in DAC internal complexity and the large number of data samples acquired per n-bit DAC [1]-[10].

Significant work has been done in the area of enhancing nonlinearity testing. Several studies proposed to reduce the number of input codes to reduce the linearity testing time. A technique was proposed to shorten the testing time by modeling a reduced order model of DAC [4]. A reduction in the number of measurement points allows for faster statistical characteristic estimation in DAC models. However, a DAC model must feature much less than 2n code of the actual DAC codes. Prior knowledge of the tested DAC error behavior also needs to be included in the model. This particular approach requires complicated mathematical simulation models of the DAC in order to define the influence of each code on its actual output voltage [10]. Also, DAC was modeled to show the effect of parasitic element and component mismatching on the converter performance [11]. However, other noise sources such as power supply and other hardware inputs were not included [7].

Others [10] proposed to reduce the number of samples by dividing the DAC input codes into segments. Each segment contains number of codes. Meanwhile, DAC output voltages, corresponding to different input codes within the same segment, are amplified to one value. This approach is based on the summation (averaging) of all output voltage values including noise. In addition, the separation of different errors can get harder as the number of bits increases. Others have focused on implementing new transformation techniques such as Wavelet Transform (WT) [2], [6], [7], [12]-[14]. The simulation with wavelets has shown improvements with satisfactory results in ADC testing. Thus, previous works in wavelet testing were applied through simulation process only using MATLAB. None of these investigators used LabView for real-time applications in ADC or DAC testing.

Since the problem of DAC testing persists due to lengthy processing delays caused by extremely large numbers of collected samples [10], the authors of this study investigated the ability of Wavelet Transform to estimate INL with fewer samples in real-time testing. Through actual testing, wavelets have shown improvements in characterizing DAC linearity error with satisfactory results. Wavelet Transform special properties of down sampling and multi-resolution allowed the reduction of compiled samples. No serious work has been done in this area to explore the actual strength of wavelet algorithms in real-time DAC testing. With the focus on shortening the testing process, reducing sample size, and simplifying testing complexity, wavelet computational efficiency was suitable for this application in contrast to the classical technique of estimating INL.

Theoretical Overview

Ideally, the DAC output voltage range is divided into equal segments, known as step size or Least Significant Bit (LSB), based on the device n-bit. In practice, the DAC voltage range is the difference between the output voltage of the lowest digital codes and the highest digital codes. By measuring the DAC voltage range or Full Scale Range (FSR) and dividing by the total number of codes, DAC unit separation step size can be stated as:

$$1 \quad LSB = \frac{Voltage[2^n - 1] - Voltage[0]}{2^n - 1} \qquad (1)$$

where "*n*" is the DAC number of bits [7], [15]-[19].

That is, for each sequence input code, the DAC analog output is incremented by exactly 1 LSB. But, in reality, distances between codes vary due to non-linearity performance of the device, as shown in Figure 1.

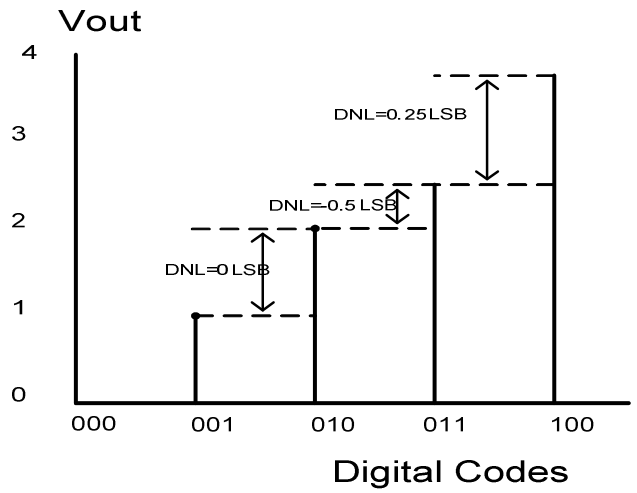

Figure 1. DAC Linearity performance in term of 1 LSB

The difference between the actual separation of adjacent individual codes and the estimated ideal step size is DNL. INL, on the other hand, is the overall linearity performance. INL measures the worst-case variation, or flatness, in the DAC analog output values with respect to an ideal straight line [15], [19]. Two straight-line methods are used in determining INL: End Point Line and Best Fit Line (linear regression). By using the End Point Line technique as shown in Figure 2, the straight line between the minimum and the maximum output value will present the ideal slope, or gain, and the INL is the deviation from this line [15]-[17].

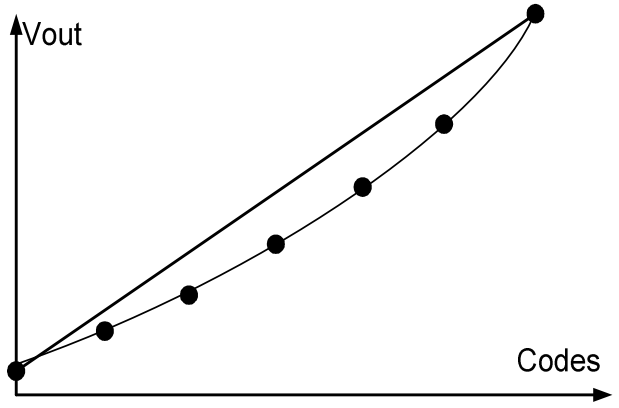

Figure 2. Endpoint Linearity Straight Line

The Best Fit Line, on the other hand, gives a representation of the DAC output linearity, based on the total sample set without looking into the smallest and largest value, as in Figure 3 [15], [16].

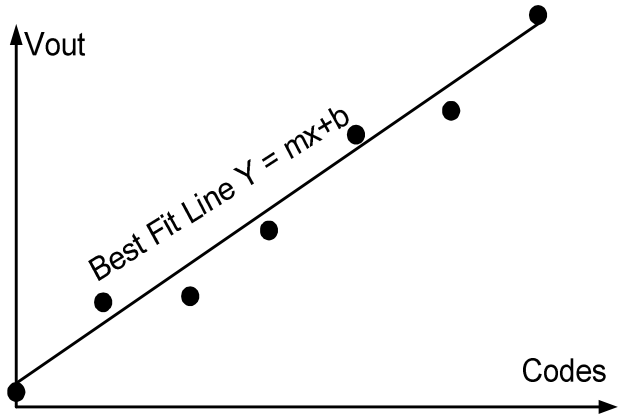

Figure 3. Best Fit Straight Line

Using either straight-line method, the INL curve can be calculated by subtracting the reference DAC straight line (End Point or Best Fit Line) from the actual output values in terms of 1 LSB. Ideally, the DAC output is linear, and the INL is equal to zero. However, in actual performance, DAC INL can be estimated as

$$INL[i] = \frac{(V[i] - V_{\mathrm{Re}f}[i])}{V_{LSB}} \qquad (2)$$

where $V[i]$ is the actual output values

$V_{\mathrm{Re}f}[i]$ is the straight line values

V_{LSB} is the measured LSB

Testing Setup

The methodology of this testing experiment, shown in Figure 4, is based on generating clean, low-frequency digital waveform codes and measuring the corresponding output voltages. This is followed by signal processing and data analysis.

Figure 4. Model setup for DAC Wavelet analysis

In this study, a pattern generator was used to produce a ramp-up digital-waveform range from (00..0) to (11..1), based on the tested DAC number of bits. Both pattern generator and Device Under Test (DUT) DAC were triggered using the same clock to determine output analog signal frequency. The continuous output waveform, in the form of a continuous voltage, was captured and digitized using a higher-bit ADC. The digitizer resolution must be at least 2 bits greater than the resolution of the DUT DAC or one quarter the LSB [16]. In this study, a 20-bit digitizer was used, which is 6 bits higher than the DUT DAC (14-bit TI DAC2904), to allow characterization and achieve a linearity measurement accuracy of 1/64 the DUT LSB. A time-domain digitized signal was transformed into the time-frequency domain using Discrete Wavelet Transform (DWT). The transform data were used in characterizing the DAC non-linearity performance, illustrated in Fast Computation Technique section.

The hardware setup shown in Figure 5 involves supplying a digital ramp signal using a National Instruments NI-PXI-6552 pattern generator. The output analog signal was captured and digitized using a NI-PXI5922 fixable resolution digitizer to measure the output analog voltage. The clock source was routed through a NI-PXI-6552 to synchronize the DUT DAC and NI-PXI5922. A low-noise power supply was used to power the DAC testing board and to provide the digital power to trigger the bits.

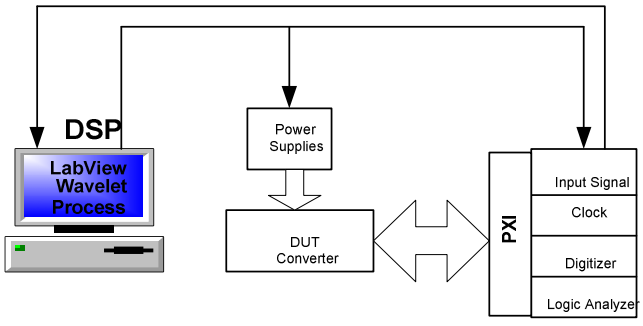

Figure 5. Experiment Hardware setup

Ramp Digital Input Codes

Non-linearity measurements were affected by the device's DC offset error, which can be caused by unsettled supply or reference-voltage input waveforms [20]. This phenomenon of unsettling requires additional time for a waveform to settle. However, testing time is often short and does not allow for settling, which may result in the DC-offset error being added to the output signal. The digital ramp signal is typically used to generate the DAC input stimulus digital waveforms and the DAC's acquired response is compared to an ideal response [16]-[20].

A computer repeatedly generates a set of ramp codes ranging from Least Significant Bit to Most Significant Bit to control a precision DAC. To eliminate waveform dead time and signal distortion, multiple ramp cycles were generated, but only one complete cycle was extracted by the digitizer. The first cycle, which could be subjected to distortion, was avoided by using derivative analysis to locate the maximum index of the derived signal and to get the starting point of the second cycle of the ramp signal.

Discrete Wavelet Transform

In most cases of signal analysis, signals are transformed and represented in a different domain. This kind of transformation, such as DWT, allows one to obtain further information in the raw signal data by localizing in frequency space and determining the position of frequency components [21], [22]. DWT is based on sub-band coding and was found to have fast computation. The computation was based on successive low-pass and high-pass filtering of the discrete time domain. Filtering was used to decompose a signal by utilizing filter banks and a down-sampling process by factor 2 (decimation) [2], [7], [22].

Assuming an output *Sn*, the new decomposed signal consists of two pieces, *Sn-1* and *dn-1* for signal approximation and detail coefficients, respectively, as shown in equations (3) and (4).

$$s_{n-1,j} = \sum_k h * s_{nk} \tag{3}$$

$$d_{n-1,j} = \sum_k g * s_{nk} \tag{4}$$

where h and g are Wavelet Transform low-pass and high-pass coefficients, respectively

Wavelet decomposition consists of two major functions: convolution and down-sampling. In down-sampling, odd-numbered coefficients are dropped and even-numbered coefficients are renumbered by inserting a "0" in place of the

removed coefficients. The notation $(\downarrow 2)a$ denotes the sequence of down-sampling by 2 as shown in equation (5).

$$((\downarrow 2)a)_k = a_{2k} \tag{5}$$

In equations (3) and (4), output signal *Sn* is convoluted with wavelets low- and high-pass coefficients, as given in equations (6) and (7)

$$(h * s_n)_j = \sum_k h * s_{nk} \tag{6}$$

$$(g * s_n)_j = \sum_k g * s_{nk} \tag{7}$$

followed by down-sampling, as given in equations (8) and (9).

$$s_{n-1} = (\downarrow 2)(h * s_n) \tag{8}$$

$$d_{n-1} = (\downarrow 2)(g * s_n) \tag{9}$$

This process of filtering and decimation at each decomposition level reduces the number of collected samples by half of the frequency band. Starting with the largest scale (the original signal), bandwidth becomes a multiple of halves at the high-pass and low-pass filters for fast algorithms of computational and implementation processes. In other words, a signal, s_n, with a frequency 100Hz, passes through the first stage of decomposition to separate the signal into two parts: high-pass and low-pass. This results in two versions of the same signal: 0-50Hz for the low-pass portion and 50-100Hz for the high-pass portion. By taking one portion or both, this process can be repeated at multiple stages. As a result, at level 2 of the high-pass decomposition, original bandwidth can be divided into 0-50Hz, 50-75Hz and 75-100Hz, as shown in Figure 6. However, if all are combined, the original signal should be observed. Therefore, DWT is easy to implement and reduces the computation time without changing the signal.

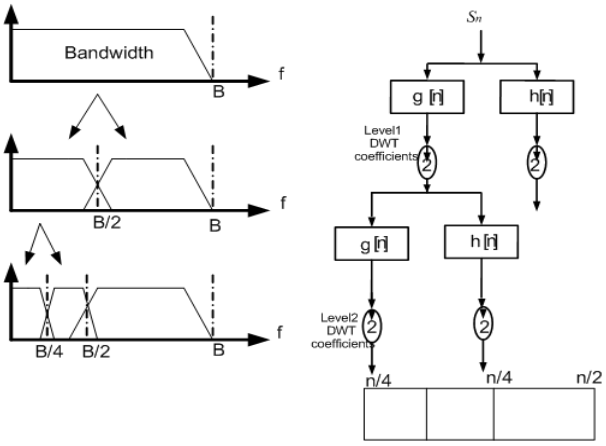

Figure 6. Wavelet Transform Multilevel Decomposition

Many types of mother Wavelets, based on the translation and scaling properties, can be used to determine signal characteristics. However, for each application, an appropriate mother Wavelet should be selected that best matches the signal [23], [24]. Selection of a specific DWT can be based on Wavelet shape, attribute, performance and signal analysis [23]. Properties of the Wavelet can be described in the time domain, (e.g., symmetry, regularity, vanishing moment, etc.), frequency domain (e.g., decaying, width of frequency window, etc.) and time-frequency domain (e.g., orthogonal, biorthogonal, fast algorithms, compact support, etc.) [23]. For example, Daubechies series are widely used in engineering applications. Using special attributes, Daubechies make conjugate quadrate filterband in multiresolotions analysis [24]. In addition, higher-order Daubechies (dbN) result in higher regularity [23]. An orthogonal wavelet with fast algorithms and computation support is a perfect match for signal spectrum analysis [23] with energy conservation.

The total energy contained in the DWT coefficients and the energy in the original signal is the same. This is suitable for signal compression and noising [21], [22]. However, unlike the orthogonal Wavelet filters (not a linear phase), biorthogonal filters can be linear-phase to allow for symmetry [21]. In this study, Haar, Coef, Daubechies (orthogonal), and biorN (biorthogonal) were used to analyze a ramp signal based on their shape characteristics, matching signal, symmetry, smoothness and phase linearity.

Fast Computation Technique

Ideally, DAC has a negligible output deviation from straight line and 0 offset voltage [15], [16]. In a non-ideal environment, a DAC analog output $\overline{x}(t)$ contains errors that distort the output signal due to noise, distortion error and heat. The output signal can be demonstrated as:

$$\overline{x}(t) = x(t) + e \tag{10}$$

where $x(t)$ = the original ramp value and
e = error-value

In this study, the DWT algorithm was applied to decompose $\overline{x}(t)$ using multi-resolution techniques and a combination of low- and high-frequency components. While low-frequency components are stationary over a period of time (approximation coefficients), high-frequency components are noisy and provide detail coefficients as shown in equations (11) and (12), respectively [21].

$$\begin{bmatrix} \vdots \\ s_{n-1,-1} \\ s_{n-1,0} \\ s_{n-1,1} \\ \vdots \end{bmatrix} = \begin{bmatrix} \cdots & \cdots & \cdots & & & & & \\ \cdots & \tilde{h}_{-1} & \tilde{h}_0 & \tilde{h}_1 & \tilde{h}_2 & \cdots & & \\ & \cdots & \tilde{h}_{-1} & \tilde{h}_0 & \tilde{h}_1 & \tilde{h}_2 & \cdots & \\ & & \cdots & \tilde{h}_{-1} & \tilde{h}_0 & \tilde{h}_1 & \tilde{h}_2 & \cdots \\ & & & & \cdots & \cdots & \cdots & \end{bmatrix} \begin{bmatrix} \vdots \\ s_{n,-1} \\ s_{n,0} \\ s_{n,1} \\ \vdots \end{bmatrix} \quad (11)$$

$$\begin{bmatrix} \vdots \\ s_{n-1,-1} \\ d_{n-1,-1} \\ s_{n-1,0} \\ d_{n-1,0} \\ s_{n-1,1} \\ d_{n-1,1} \\ \vdots \end{bmatrix} = \begin{bmatrix} \cdots & \cdots & \cdots & & & & & \\ \cdots & \tilde{h}_{-1} & \tilde{h}_0 & \tilde{h}_1 & \tilde{h}_2 & \cdots & & \\ \cdots & \tilde{g}_{-1} & \tilde{g}_0 & \tilde{g}_1 & \tilde{g}_2 & \cdots & & \\ & \cdots & \tilde{h}_{-1} & \tilde{h}_0 & \tilde{h}_1 & \tilde{h}_2 & \cdots & \\ & \cdots & \tilde{g}_{-1} & \tilde{g}_0 & \tilde{g}_1 & \tilde{g}_2 & \cdots & \\ & & \cdots & \tilde{h}_{-1} & \tilde{h}_0 & \tilde{h}_1 & \tilde{h}_2 & \cdots \\ & & \cdots & \tilde{g}_{-1} & \tilde{g}_0 & \tilde{g}_1 & \tilde{g}_2 & \cdots \\ & & & & \cdots & \cdots & \cdots & \\ & & & & \cdots & \cdots & \cdots & \end{bmatrix} \begin{bmatrix} \vdots \\ \vdots \\ \vdots \\ s_{n,-1} \\ s_{n,0} \\ s_{n,1} \\ \vdots \\ \vdots \\ \vdots \end{bmatrix} \quad (12)$$

From the high-pass filter, detail coefficients were obtained as indicated in equation (13) and down-sampled by 2, taking the odd values as shown in (14), to end with half of the original data.

$$(..d_{n-1,-1}d_{n-1,0},d_{n-1,1},d_{n-1,2},d_{n-1,3},d_{n-1,4},d_{n-1,5},d_{n-1,6},d_{n-1,7},..) \quad (13)$$

$$(...d_{n-1,-1},d_{n-1,1},d_{n-1,3},d_{n-1,5},d_{n-1,7},...) \quad (14)$$

The collected detail coefficients in the first multi-resolution were used again for a second-level multi-resolution by repeating equations (12)-(15), as shown in Figure 7.

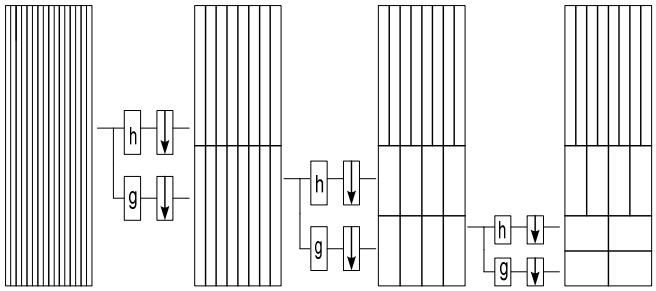

Figure 7. Data decomposition process

To compute INL using DWT coefficients, high-pass coefficients at the 2nd stage of multi-resolution were used. As in the case of computing instantaneous DNL [2], [7], instantaneous magnitudes of the high-pass filter at the 2nd level of data decomposition were used in place of the original codes for INL estimation, where codes in the time-frequency domain represented a different version of the same signal.

By applying DWT coefficients into the INL estimation, the INL was determined by subtracting the reference calculated straight line (based on instantaneous magnitudes) from the instantaneous magnitudes, and normalized by the DUT Δ_{ideal}. As a result, the instantaneous INL can be computed as:

$$INL(n) = \frac{\max\left\{\left|\left|d_n\right| - \left|d_{ref(n)}\right|\right|\right\}}{\Delta_{ideal}} \quad (16)$$

where Δ_{ideal} is ideal LSB

d_n is instantaneous magnitudes

$d_{ref(n)}$ is corresponding straight-line magnitudes

Experimental Results

The proposed algorithm was implemented in LabView because of its proficiency in testing control, automation, and data acquisition [25]. A picture of the arranged bench prototype testing setup is shown in Figure 8. Testing setup consists of: 1) a National Instrument PXI 1042, capable of generating various analog and digital waveforms, built-in clock synchronization, high-resolution digitizer, and built-in logic analyzer; 2) device-under-test DAC; and, 3) PC terminal for testing engineering interfaces and interpolation of testing results.

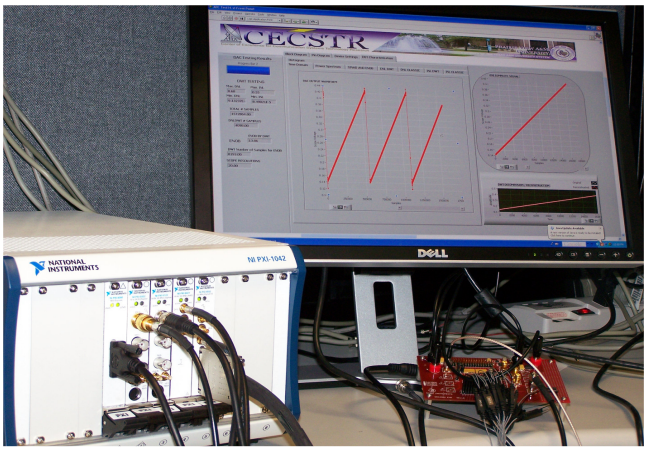

Figure 8. Bench Prototype Testing Setup

INL testing uses the classical technique as shown in Figures 9, 11 and 13 for 14-bit, 12-bit, and 10-bit DACs, respectively. Meanwhile, Figures 10, 12, and 14 illustrate the proposed DWT INL testing for 14-bit, 12-bit, and 10-bit DACs, respectively.

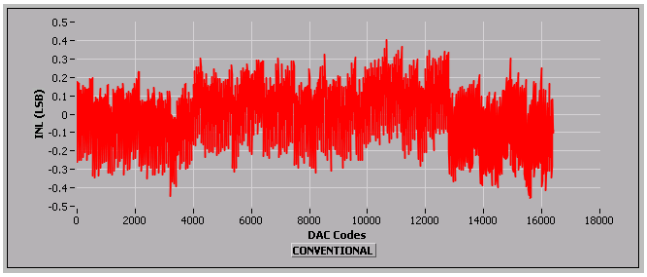

Figure 9. 14-bit DAC INL Computation

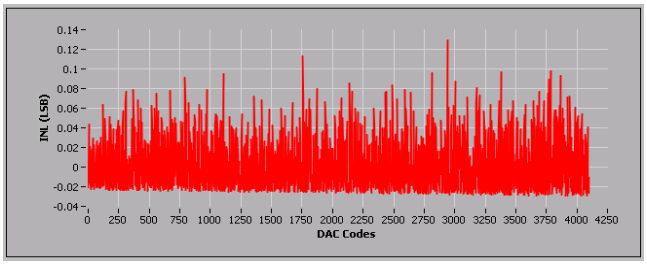

Figure 10. 14-bit INL Wavelet Based Computation

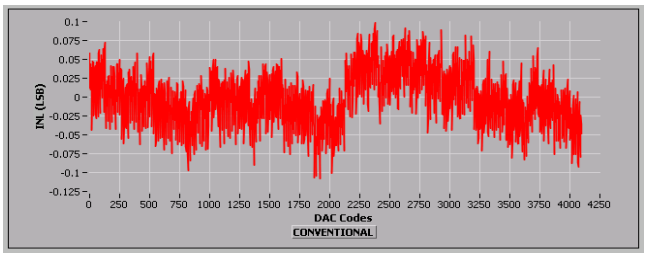

Figure 11. 12-bit DAC INL Computation

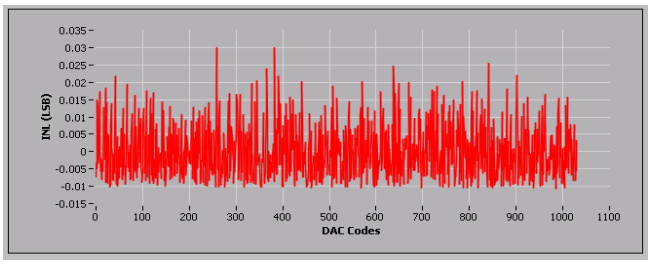

Figure 12. 12-bit INL Wavelet Based Computation

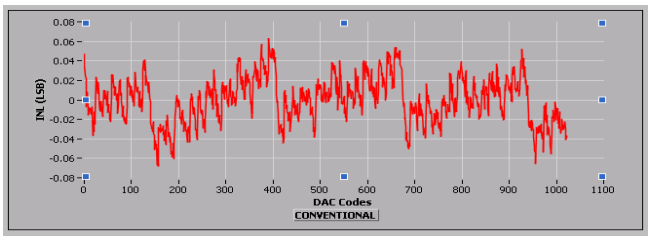

Figure 13. 10-bit DAC INL Computation

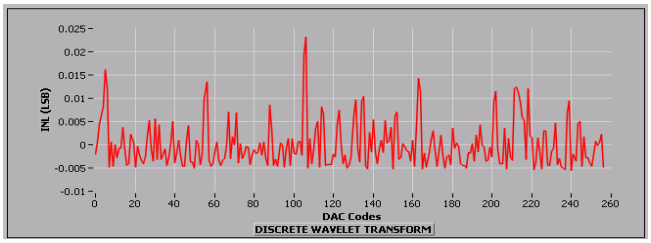

Figure 14. 10-bit INL Wavelet-Based Computation

As shown in Figures 7 and 8, for example, in classical testing of 14-bit DAC, a total of 16,383 codes were used in estimating the maximum INL, while in the DWT testing algorithm, 4,099 codes were used. In Figures 9 and 10, for the 12-bit DAC, a total of 4,095 codes were used in classical testing and 1,032 codes in the DWT algorithm. Also, for the 10-bit DAC in Figures 11 and 12, 1,023 codes were used in computing the INL, while 258 were used in the DWT algorithm. This significant reduction in the number of codes and shortened INL computation was due to the special DWT properties of dilatation and translation that allows Wavelet to zoom into signal data information, prevent redundant information during decomposition, and to possess the same amount of energy contained in the original data for signal reconstruction [21], [22].

To validate these experiment results, testing was performed using several clock frequencies and DWT mother wavelets. Results were validated with classical testing as well as device specifications as shown in Tables 1- 3 and Figures 15-17.

Table 1. INL estimation for 14-bit (DAC2904, TYP INL = ± 5)

Fclock (KHz)	C.T	db4	db2	Haar	Bior3-1	Coef1
100	0.47	0.16	0.12	0.14	0.41	0.11
150	0.42	0.11	0.13	0.13	0.46	0.13
200	0.46	0.13	0.17	0.13	0.4	0.11

C.T – Classical Testing

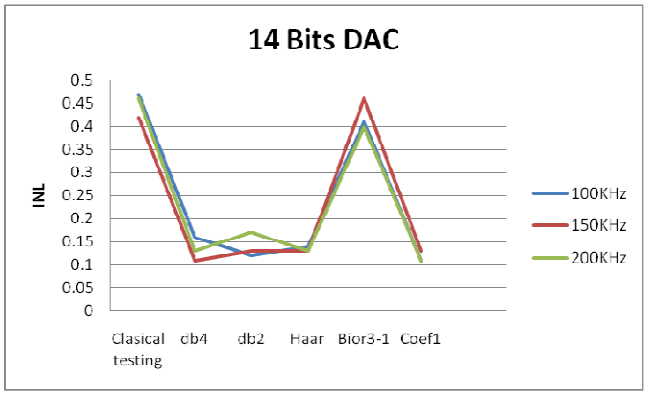

Figure 15. Illustration of INL values from Table 1

Table 2. INL estimation for 12-bit (DAC2902, Typ INL = ±3)

Fclock (KHz)	C.T	db4	db2	Haar	Bior3-1	Coef1
100	0.16	0.03	0.08	0.03	0.22	0.07
150	0.18	0.04	0.06	0.04	0.21	0.06
200	0.17	0.04	0.06	0.04	0.21	0.06

C.T – Classical Testing

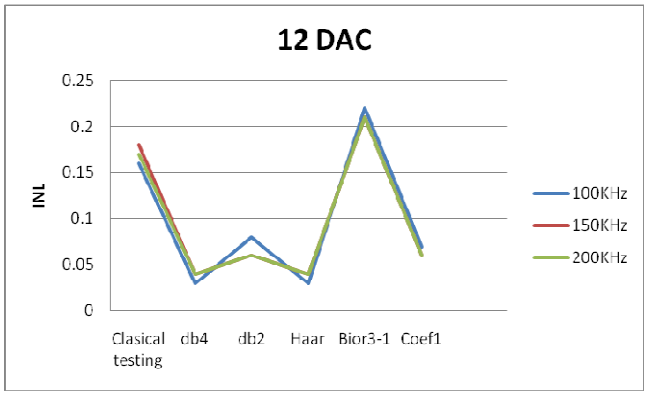

Figure 16. Illustration of INL values from Table 2

Table 3. INL estimation for 10-bit (DAC2900, Typ INL = ±1)

Fclock (KHz)	C.T	db4	db2	Haar	Bior3-1	Coef1
100	0.08	0.01	0.03	0.02	0.11	0.03
150	0.09	0.01	0.03	0.03	0.1	0.02
200	0.09	0.02	0.05	0.02	0.15	0.02

C.T – Classical Testing

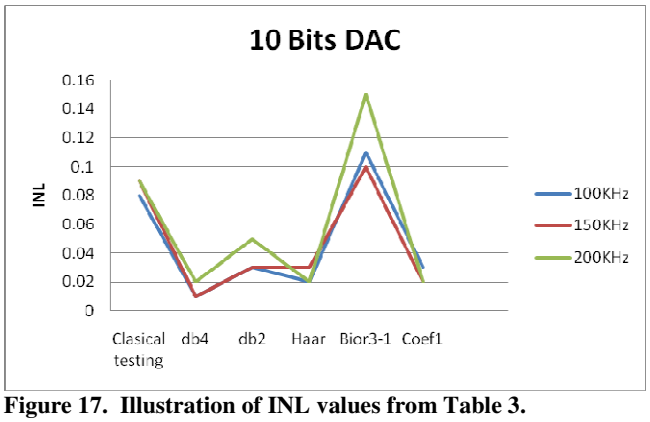

Figure 17. Illustration of INL values from Table 3.

Discussion

The Wavelet Transform showed improvements in testing INL by reducing the number of sampling data and computational complexity. As indicated in the testing process, Wavelet Transform algorithms reduced the amount of compiled data by 75% of collected data samples, which reduces the data-storage space requirements by the same amount, and shortens test duration from 312ms in conventional testing to 134ms using Wavelet algorithms.

The selection of the Wavelet was based on the Wavelet shape characteristics, matching signal, orthogonality, and filter linearity. As seen from Tables 1, 2 and 3, bior3-1 outperformed Haar and dbN Wavelets, due to the matching signal characteristics of the ramp-up signal and linear-phase filters.

Conclusion

A new method of testing INL mixed-signal DACs was presented to show the ability of DWT in analyzing output signals, and identify bit errors due to signal distortions, noise, and DC offset, that can be integrated into the output signal. This method of testing can be implemented in testing other DAC parameters such as gain and DC offset error. The benefit of Wavelet algorithms in decreasing the number of sample data can be used for a faster testing process, decreased cost, and more accurate results. DWT can be especially suitable for the incredible growing demands for high-speed, high-resolution converters, built-in self-test algorithms, and self-calibration schemes.

References

[1] E. Balestrieri, P. Daponte, S. Rapuano, "Recent developments on DAC modeling, testing and standardization Measurement", ELSEVIER , 9th Workshop on ADC Modeling and Testing, April 2006, pp. 258-266.

[2] T. Yamaguchi, M. Soma, "Dynamic Testing of ADCs Using Wavelet Transform" in 1997 Proc. IEEE Test Conf., pp. 379-388.

[3] F. Adamo, F. Attivissimo, N. Giaquinto, A. Trotta, "A/D converters nonlinearity measurement and correction by frequency analysis and dither" IEEE Trans. Instrumentation and Measurement, Aug 2003. pp. 1200 – 1205.

[4] B. Vargha, J. Schoukens, Y.; Rolain, "Using reduced-order models in D/A converter testing" in 2002 Proc. IEEE Instrumentation and Measurement Technology Conf., pp.701-706.

[5] J.T. Doyle,L. Young; K. Yong-Bin, "An accurate DAC modeling technique based on Wavelet theory" In 2003 Proc. IEEE Custom Integrated Circuits Conf., pp. 21-24.

[6] R. O. Marshall, C. M. Akujuobi, "On the Use of Wavelet Transform in Testing for the DNL of ADCs", In Midwest Symposium, 2002. IEEE Circuits and Systems, pp. 25-8.

[7] C.M. Akujuobi, E. Awada "Wavelet-based differential nonlinearity testing of mixed signal system

ADCs"; In 2007 Proc. IEEE Southeast Conf., pp. 76 – 81.
[8] S. Cherubal, A. Chatterjee, "Optimal linearity testing of analog-to-digital converters using a linear model" IEEE Trans. Circuits and Systems I: Mar 2003, pp.317 – 327.
[9] Y. Cong; R.L. Geiger, " Formulation of INL and DNL yield estimation in current-steering D/A converters ",IEEE International Symposium on Circuits and Systems, 2002, pp. III-149
[10] B. Vargha, J. Schoukens, Y. Rolain, "Static nonlinearity testing of digital-to-analog converters" IEEE Trans. Instrumentation and Measurement, Oct 2001, pp. 1283 – 1288.
[11] J.J. Wikner, N. Tan, "Modeling of CMOS digital-to-analog converters for telecommunication" IEEE Trans. Circuits and Systems II: May 1999, pp. 489 – 499.
[12] C. M. Akujuobi, L. Hu, "A Novel Parametric Test Methods for Communication System Mixed Signal Circuit Using Discrete Wavelet Transform", IASTED, St. Thomas, US Virgin Island, Nov 2002.
[13] C. M. Akujuobi, L. Hu, "Implementation of the Wavelet Transform-based Technique for static Testing of Mixed Signal System", IASTED, CA. Palm Spring, US, Feb 2003.
[14] A. Gandelli, E. Ragaini, "ADC Transfer Function Analysis by Means of A Mixed Wavelet-Walsh Transform" in 1996 Proc. IEEE Instrumentation and Measurement Technology, pp. 1314 – 1318.
[15] M. Baker, " Demystifying Mixed Signal Test Methods". Newnes, Elsevier Science, 2003, pp. 147-237.
[16] M. Burns, G. W. Roberts "An Introduction to Mixed-Signal IC Test and Measurement", Oxford University Press, New York, 2004, pp. 159-527.
[17] J. Paul "Integrated Converters", Oxford University Press, New York, 2001, pp. 1-27.
[18] B. Razavi "Data Conversion System Design", Wiley-Interscience, Newyork, 1995, pp 45-70.
[19] IEEE Standard 1241, IEEE Standard for terminology and test methods for analog-to-digital converters, 2000.
[20] J. Schat, "Testing low-resolution DACs using the Generalized Morse Sequence as Stimulus Sequence for Cancelling DC drift". in 2007 International; Conf. IEEE Circuits and Systems, pp. 371-374.
[21] F. Keinert "Wavelet and Multiwavelets", Chapman and Hall, Baca Raton, FL. 2004, pp39-67.
[22] O. Riouel, M. Vetterli, " Wavelet and Signal Processing," IEEE SP Mag., Volume 8, No. 4, pp. 14-38, Oct. 1991.
[23] L. Peng, D. Jian-dong "Characteristic Analysis and Selection of Wavelets Applicable for Ultra-High-Speed Protection" in 2005 IEEE Conf. Transmission and Distribution, pp 1-5.
[24] Y. Qing-Yu; H. Mu Long, W. Li-Yan, "Fault Line Detection of Non-Effectively Earthed Neutral System Based on Modulus Maximum Determining Polarity" in 2009 IEEE Conf. Power and Energy, pp 1-4.
[25] C.M. Akujuobi, E. Awada,"Wavelet-based ADC Testing Automation Using LabView";. International Review of Electrical Engineering Transaction, Vol 3, pp. 922-930, Oct 2008.

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