DEVELOPMENT OF A COMPACT THREE-PHASE INDUCTION MOTOR DRIVE SYSTEM WITH DISCRETE COMPONENTS

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Abstract

Growth in the high-volume market in variable-speed drives (VSDs) is expected due to emerging applications in both home appliances and process industries. VSDs greatly improve efficiency in those applications. Almost all of these applications do not require precise positioning or speed control and, hence, are of low-performance types. The inverter-controlled induction motor drive (IMD) is a strong competitor for such applications due to the low-cost of the motor and its inherent features such as simplicity of control requiring no sensors in these low-performance applications. It is brushless, as it has no slip rings, thus making it truly almost maintenance-free and robust.

This study addresses issues of design and development of such a low-cost inverter and its controller in order to obtain a one-horsepower variable-speed IMD. In addition, an implementation of VSD with analog and discrete components is thoroughly discussed. The various issues addressed in detail are: specifications, appropriate control strategy and drive configuration, design of control circuits, and their switching and conduction losses and tuning. Results from a fully-tested one-horsepower experimental inverter-controlled induction motor drive system are presented to correlate the key design aspects and design specifications. The proposed VSD for the three-phase induction motor is implemented mostly with analog and discrete components; it will be very useful to students in electric motor drive courses to get an insight into a three-phase inverter and hands-on experiences in building and testing such a system.

Introduction

Emerging high-volume VSD applications have the stringent requirements of low-cost and compact packaging for the electronic inverter and its controller to induce the conversion of many fixed-speed applications to VSD operations with very little added cost due to the extra electronic components. The presentation of various studies would enhance the design and development concepts leading to the achievement of low-cost and compact drives for the motor drives market.

Such a study of the design and development of a one-horsepower inverter and its controller for an IMD achieving the specified requirements is presented in this paper. Furthermore, the proposed VSD for the three-phase induction motor is implemented mostly with analog and digital discrete components to gain insight into a three-phase inverter system and hands-on experience in building and testing a VSD for electric motor drives courses.

The induction motor is essentially a constant speed machine if a constant voltage and frequency source is connected [1]. When the load torque increases, the induction motor speed drop will be minimal, which is the advantage for constant-speed applications. Many single-chip microprocessor or digital signal controller (DSC) solutions to design a three-phase inverter for induction-motor-based VSDs involve a lot of software design; thus, they are not suitable solutions for this study [2], [3]. However, the software control of a VSD is desirable for providing flexibility of control and tuning without tinkering with hardware components, but it may not be sufficient to deal with details of VSD system implementation without a background in specific software language programming skills. The exposure of the major functional subsystems of the VSD to students is very important to the understanding of the overall system requirements and the design circuitry to meet the system requirements. The design philosophy in this study was to use as many commercial off-the-shelf (COTS) discrete analog and digital components as possible in order to provide rich insight into the IMD system and plenty of hands-on opportunities for the students to understand, analyze, and build it [3-15].

The highlights of this study are as follows: The specifications of the drive system and the rationale for choosing a drive system control strategy are explained first. Then, the subsystems of the proposed IMD are functionally identified. The design concepts of various subsystems and their implementation are explained. The outlines of the drive losses which lead to the selection of cooling arrangement satisfying the cost and packaging requirements are explained. The layout and final assembly of the power and control circuits are described along with the packaging details including that of the enclosure. Experimental results from the prototype inverter-fed IMD are presented to validate the design and conformity to specifications. In

conclusion, various teaching topics for electric motor drives courses are suggested, based on the proposed IMD system.

Drive System Specifications and Selection of a Control Strategy

System Specifications

The induction motor considered for the development of the inverter and its controller was one-horsepower with three-phase windings and two poles, even though the number of poles does not affect the general design and development approach outlined in this paper. The ac input available was single-phase either with 50 or 60Hz and 240V. The design was modifiable for 120Vac input, hence the power rating of the inverter, without any modification, may be considered as 0.5hp.

The following general requirements and desirable features are the starting points for consideration of an IMD system design strategy: first quadrant operation capability, which means motoring operation only, variable stator voltage and variable stator frequency (VVVF), variable voltage with pulse-width modulation (PWM) at a low frequency to enhance efficiency of the overall IMD system, soft starting, current-limiting feature for the protection of the inverter, variable PI speed-controller gains, and provision for operation with and without tachogenerator feedback. In addition to these requirements, the following specifications, summarized in Table 1, were considered satisfactory for fan/pump types of loads.

Table 1. Target Specifications of the Proposed IMD

Power Source	Single-Phase, 240Vac, 50/60Hz
Output Power	1-hp maximum, three-phase
Output Voltage Range	0 to 220Vrms (line-to-line)
Output Frequency Range	0.1 to 86Hz
Commanded Speed Reference Voltage	5V for the rated speed
Measured Speed Input Voltage	50V maximum at rated speed
Modulation Method	Sine-triangular PWM (SPWM)
Carrier Frequency	2.78kHz
Protection Features	Current and torque limitation with undervoltage operation prevention
Adjustments	Soft start controller time constant, proportional and integral speed controller gains, torque limit, offset voltage, V/Hz ratio, and dc bus current limit
Ambient Temperature	0 to 40°C (70°C with derated output power)
Cooling Method	Forced air cooling
Target Package Volume	100 cubic inches

The parameters of the single-phase equivalent circuit of an induction motor are obtained by these measurements [1]: After running the motor until it was warmed up, the stator resistance, R_s, was determined from three dc resistance measurements between each pair of motor phases, and the obtained data were averaged and divided by two.

Other measurements were undertaken with the no-load test at the synchronous speed (3,600rpm) and the locked-rotor test at rest. The induction motor ratings and measured and calculated parameters are listed in Table 2.

Table 2. Induction Motor Ratings and Measured Parameters

Ratings of the Induction Motor under Test	1-hp, 230V, 3 phase, 60Hz, 3A, 3450rpm, 2-pole, Y-connected
Measured and Calculated Induction Motor Parameters at 60 Hz	R_s=2.355Ω, R_r=2.055Ω, L_m=183.4mH, L_{ls}=L_{lr}=7.388mH

Selection of a Drive Control Strategy

Based on the drive specifications, the most important first step is to identify the appropriate control strategy for the inverter-fed induction motor drive. The volts-per-hertz (V/Hz) control strategy was selected because it has sufficient performance from the point of view that it requires simple control circuitry [1]. It keeps the flux magnitude in the motor approximately constant by maintaining the voltage-to-frequency ratio constant except for a small resistive voltage offset. It is also not dependent on feedback signals for open-loop operation, requires very simple tuning in the form of its offset trimming and the change of voltage-to-frequency ratio.

As the frequency decreased at low speed, the voltage drop across the stator resistance can no longer be neglected; thus, an offset or boost voltage is necessary to provide the rated flux at low speeds. The effect of the offset voltage is negligible at higher frequencies. That even stator current measurement and feedback are not essential to this strategy is an important factor to be noted. All other control strategies, such as vector control, constant air gap flux control, and slip control, involve a greater use of control circuitry and feedback sensors, though they offer much more precise control of torque and speed. Since these control strategies involve rigorous code development efforts with a microprocessor or DSC, they were, therefore, not considered in this study in order to implement a simple controller with discrete analog and digital components.

Overall Drive System

The simplified block diagram of the proposed IMD incorporating the V/Hz control strategy is shown in Figure 1. The speed reference, ω_m^*, is processed through a soft-start circuit, whose time constant can be adjusted externally with a potentiometer. The output of the soft-start circuit provides the modified speed command from which the filtered speed feedback signal is subtracted to provide the speed error. The speed error is amplified and processed through a proportional-plus-integral (PI) controller resulting in the
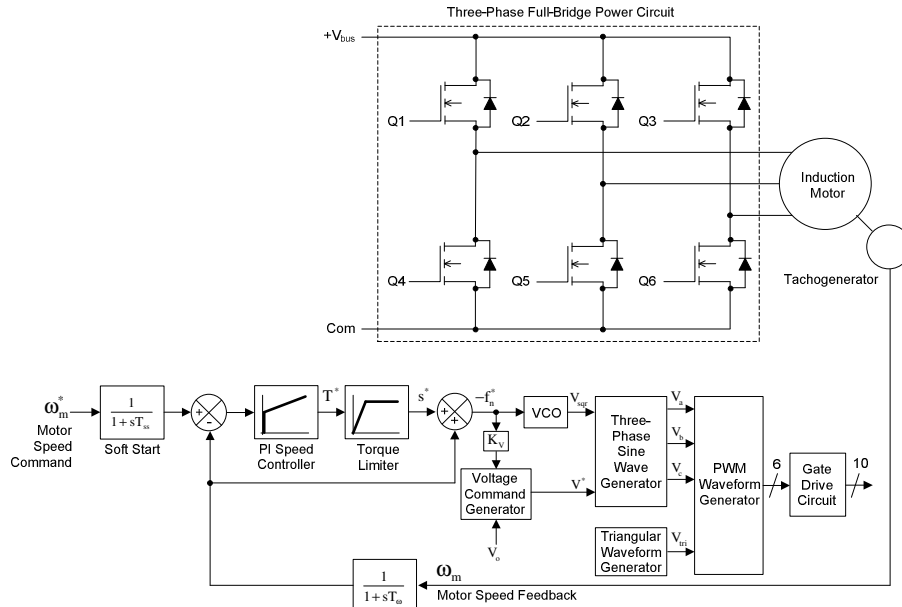
Figure 1. Block diagram of the proposed IMD incorporating the constant V/Hz technique

torque command, T^*, which is further processed through a torque limiter. The torque limiter constrains the torque to be within the stable region of the steady-state torque slip region and, in the process, also limits the currents to be within the permitted levels.

In the stable operating region the torque is proportional to the slip speed; hence, the output of the torque limiter could be taken as slip speed command, s^*. The slip speed command is added to the filtered normalized rotor speed, obtaining the normalized stator angular speed command or normalized stator frequency command, f_n^*. The stator frequency is multiplied by the voltage-to-frequency ratio and added to the stator offset voltage, V_o, to provide the stator voltage command. The offset voltage is intended to overcome the reduction of the air gap voltage and, hence, in the weakening of the magnetizing current due to the large stator resistive voltage drop at low speeds.

The stator frequency and voltage commands are then fed to a sine wave generator block to generate the three-phase stator voltage commands. These phase voltage commands are translated to actual phase voltages through SPWM with a triangular carrier frequency and obtaining a set of gate drive signals to the inverter bridge. The dc input voltage to the inverter is obtained through a diode full-bridge rectifier fed from a single-phase ac supply. It can be any dc voltage source, such as a solar panel and a wind generator with or without a front-end boost converter to control the dc bus voltage level.

Drive System Design and Realization

Design of an IMD System

The various major subsystems shown in Figure 1 were considered for design and implementation in this section. The schematic of each block and the realization with discrete analog and digital components may lead to application-specific integrated-circuit (ASIC) packaging if this design is to be adopted for manufacturing. But at this stage of prototype verification, it was decided to avoid the costs associated with such a development. Furthermore, the implementation of such a drive system with a microprocessor is not an option in this study to provide an insight of the drive system, which consists of discrete components only. Either a microprocessor (microcontroller) or DSC solution to implement a drive system usually involves a significant software development effort.

For the PWM signal generation in this study, the sine-triangular carrier modulation method was selected due to its simplicity for implementation. It consists of a carrier wave, which is basically a high-frequency triangular waveform, and a sinusoidal modulation signal, whose amplitude varies depending on the speed command. These two signals were compared to generate a desired PWM output. The width of each PWM pulse is weighted by the amplitude of the sine wave at that instant. Therefore, the rms value of the voltage applied to the motor phase can be controlled by varying the duty cycle of the PWM signal. A voltage of 5V is selected to represent 1 p.u. value.

Soft-Start Circuit

The developed soft-start circuit consists of a difference amplifier (IC1:D) and an integrator (IC1:C). They are cascaded together to get a slow-rising voltage ramp. Figure 2 shows the soft-start circuit and has a transfer function of
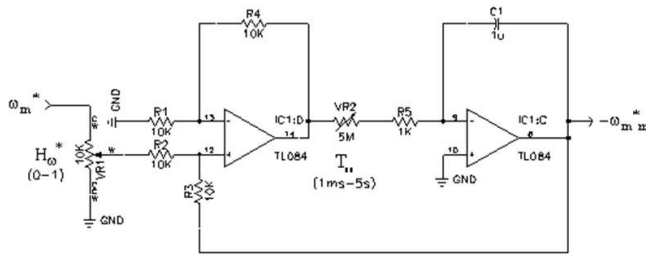
Figure 2. Soft-start circuit

$$G_{ss}(s) = \frac{1}{1 + T_{ss} \cdot s} \tag{1}$$

where

$$T_{ss} = (VR2 + R5) \cdot C1 \tag{2}$$

is the soft-start time constant that can be varied with VR2 from 1ms to 5s. VR1 adjusts the commanded normalized speed input gain, H_{ω}^{*}. When VR1 is turned to its maximum position, the 5V input commands the rated speed. In order to command the rated speed with a higher voltage, VR1 should be decreased accordingly.

PI Speed Controller

The PI speed controller shown in Figure 3 consists of IC2:C and IC2:D. Its transfer function is

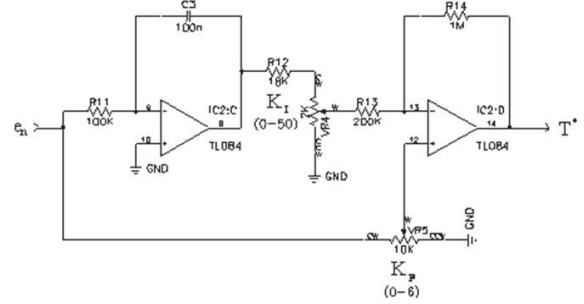$$G_{c}(s) = K_{P} + \frac{K_{I}}{s} \tag{3}$$

Figure 3. PI speed controller circuit

It produces the torque command, T^{*}. VR5 varies the proportional gain, K_{P}, from 0 to 6, and VR4 varies the integral gain, K_{I}, from 0 to 50. Since there is no simple way to determine these gains with the motor parameters, they should be adjusted empirically.

Torque Limiter

The torque limiter limits the torque and, consequently, the motor current to a safe level and prevents the motor from operating in the unstable region. The implemented torque limiter circuit is shown in Figure 4. It is formed around IC2:B and IC2:A. D1 does not allow the input voltage to exceed the voltage at the wiper of VR6, and, therefore, VR6
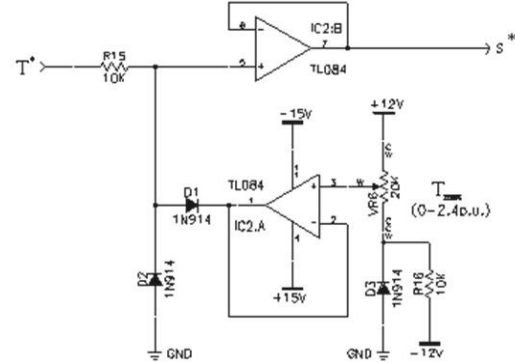
Figure 4. Torque limiting circuit

adjusts the torque limit from 0 to about 2.4 p.u.. D2 does not allow negative input voltages, since this is a one-quadrant drive and torque cannot be negative. The torque is proportional to the slip; the output of this circuit is the commanded slip speed in a normalized unit, s^{*}.

Voltage Command Generation Circuit

The voltage command generation circuit is implemented with an inverting amplifier IC3:B and is shown in Figure 5.
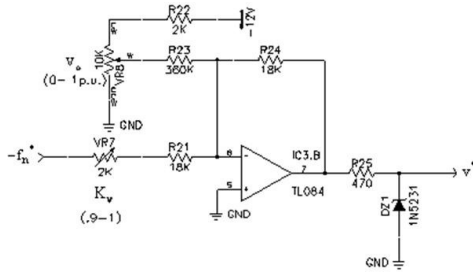
Figure 5. Voltage command schematic

It produces the commanded normalized voltage from the commanded normalized synchronous frequency using the formula

$$v^* = v_o + K_v \cdot f_n^* \qquad (4)$$

where v_o is the normalized offset voltage and K_V is the normalized frequency to normalized voltage constant. VR8 varies v_o from 0 to 0.1 p.u., and VR7 varies K_V from 0.9 to 1. At the output of this block, there is a 5.1V zener diode, which prevents commanded voltages higher than the rated level of 5V. This causes the motor to operate in the flux-weakening region for speeds higher than the rated one.

Voltage-controlled Oscillator

Figure 6 shows the voltage-controlled oscillator (VCO), which is implemented with IC4 (XR 2207). The difference amplifier consists of IC3:C, and IC3:D brings the input voltage to a value suitable for IC4. This block produces a TTL level square wave, v_{sqr}, with a frequency of f_a given by
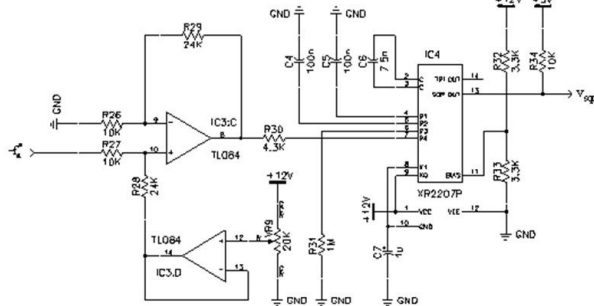

Figure 6. VCO schematic

$$f_a = \frac{1}{R31 \cdot C6} \cdot \left[1 - \frac{(V_c - 6) \cdot R31}{6 \cdot R30} \right] \qquad (5)$$

where V_c is the voltage at the output of IC3:C, and is given by

$$V_c = 2.4 \cdot V_{in} + 12 \cdot \frac{VR9_W}{VR9} \qquad (6)$$

where $VR9_W$ is the resistance from the pot wiper to its end. VR9 adjusts the frequency to be 1024 times the commanded value.

Three-Phase Sine Wave Generation Circuit

The three-phase sine wave generation circuit produces three-phase sinusoidal waveforms according to the commanded normalized synchronous frequency and the commanded normalized voltage. Figure 7 shows the sine wave generator block.

The signal from the VCO feeds a 12-stage ripple counter, IC5. The outputs of the counter's first ten stages, or $1024 = 2^{10}$, form a 10-bit address bus for a 16-bit output EPROM, IC6, where the sine waves for phases A and B are stored with 8-bit resolution for each phase. IC7 and IC8 are multiplying 8-bit DACs that produce negative voltages down to -5V. The amplitude and offset of the generated sine waves vary according to the commanded voltage signal so that
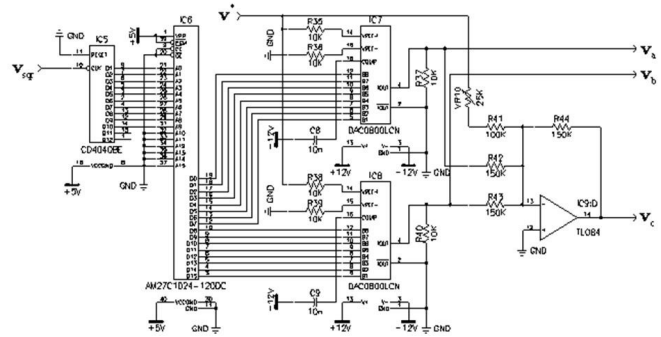

Figure 7. Sine wave generator circuit

$$v_a = -v^* \cdot \frac{1 + sin(2\pi \cdot f_s^* \cdot t)}{2} \qquad (7)$$

$$v_b = -v^* \cdot \frac{1 + sin(2\pi \cdot f_s^* \cdot t - \frac{2\pi}{3})}{2} \qquad (8)$$

where f_s^* is the commanded synchronous frequency. The voltage for the phase C is produced from the inverted summing amplifier circuit with IC9:D, as

$$v_c = -\tfrac{3}{2} v^* - (v_a + v_b) \qquad (9)$$

VR10 balances the three-phase system eliminating any undesirable offset voltage from IC9:D.

Triangular Waveform Generation Circuit

The three-phase inverter was designed to operate at a switching frequency of $f_S = 2.78\text{kHz}$. Therefore, the output of a carrier frequency generation circuit has the same frequency. Figure 8 shows the triangular carrier waveform generator circuit, which is formed around IC11.
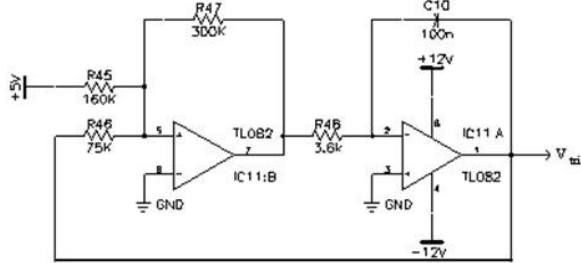

Figure 8. Triangular wave generator schematic

This circuit produces a triangular waveform, v_{tri}, with a frequency of f_b, which is given by

$$f_b = \frac{R47}{4 \cdot R46 \cdot R48 \cdot C10} \tag{10}$$

And has a peak-to-peak amplitude, V_m, given as

$$V_m = 2 \cdot V_{max} \cdot \frac{R46}{R47} \tag{11}$$

where V_{max} is the maximum output voltage of IC11 with 10V, and an offset of V_{of}

$$V_{of} = 5 \cdot \frac{R46}{R45} \tag{12}$$

which matches the output voltage range of the DAC0800.

Three-Phase PWM Generation Circuit

Figure 9 shows the three-phase PWM block comprised of IC10, IC9:B and IC9:C. Each of the three-phase sine waves is compared with the common triangular carrier waveform with two complementary comparators to produce the three-phase PWM signals: IC10:C and IC10:B for v_a, IC10:D and IC10:A for v_b, and IC9:C and IC9:B for v_c. The outputs of the comparators are v_{L1} - v_{L3} for the low-side and v_{H1} - v_{H3} for the high-side drive signals for the succeeding gate drive circuit.
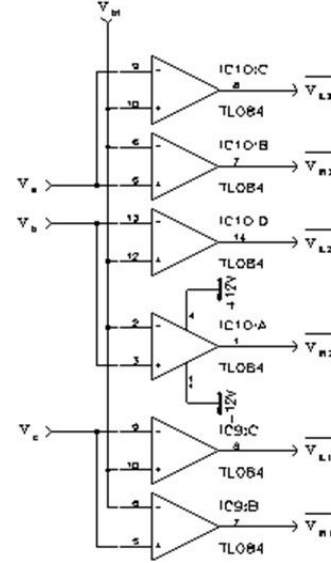

Figure 9. Three-phase PWM generation circuit

The Multisim circuit diagram for the simulation of the SPWM technique is shown in Figure 10. The schematic diagram shows the single phase only. The triangular carrier signal is common to all three-phase PWM generation circuitry. R1 and R2 are dummy loads to monitor resulting PWM signals. The simulation result which depicts the three-phase SPWM technique is shown in Figure 11(a) with the three-phase sine waves and triangular carrier waveform. The generated high-side PWM signal for the following gate drive IC, IR2130, is shown in Figure 11(b).
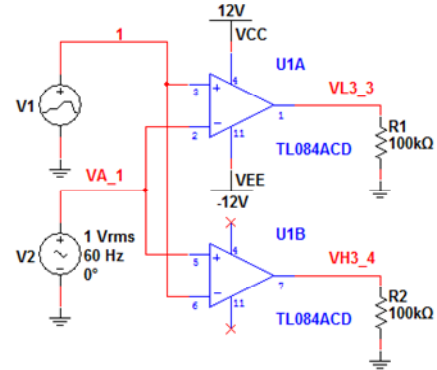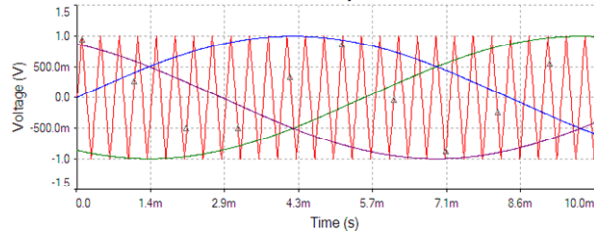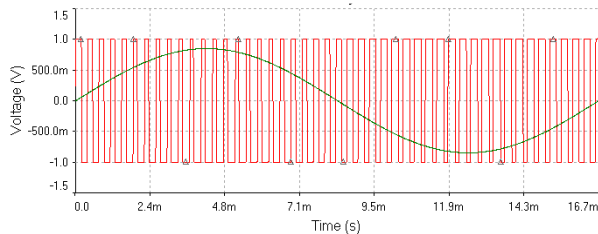

Figure 10. Multisim three-phase SPWM generation circuit (single phase only)

(a) Multisim simulation result with three-phase sine waves (60 Hz) and triangular carrier waveform (2.78 kHz)

(b) Three-phase SPWM signal for the phase A

Figure 11. Multisim simulation result of the normalized three-phase PWM signals with SPWM technique

Gate Drive Circuit

A high-voltage three-phase gate driver IC, IR2130 from International Rectifier, is used for interfacing gate drive signals with MOSFET power switches. Figure 12 shows the gate drive circuit which is implemented with IC12 (IR 2130). The PWM signals are limited to a 0-5V range, and fed to the gate driver circuit, IC12, which interfaces them to the power-switching devices. IC12 contains three floating and three ground-referenced drivers, and provides dead time between the high and the low sides, as well as current limiting. VR11 adjusts the dc bus current limit value from 2A. It should be adjusted so that the instantaneous bus current does not exceed the rated instantaneous switching power device current. v_{G1} - v_{G6} are
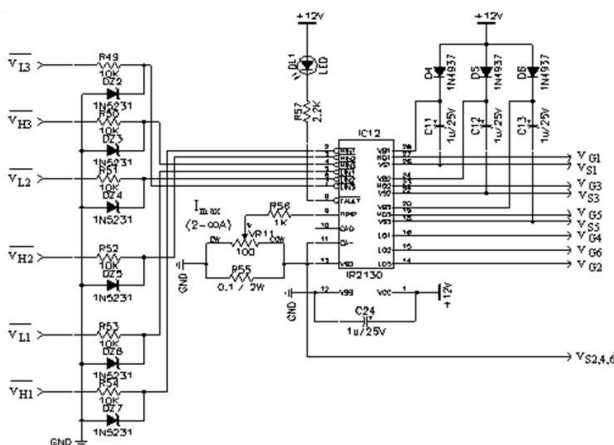

Figure 12. Gate drive circuit

connected to the gate terminals of the power switching devices, and v_{S1} - v_{S6} to the power devices' source terminals. In this study, the three-phase inverter circuit consists of six IRF840 Power MOSFET devices. But integration of those power devices by replacing them with an intelligent power module, which encases the dedicated gate drive circuit and protection circuit, may provide better thermal management, a smaller footprint, and less electromagnetic interference (EMI) noise emission.

Loss Evaluations and Cooling Design

Losses in the Converters

The inverter operates at a switching frequency of f_S = 2.78kHz. The resistors that are in series with the devices' gates set the switching time to about 0.5μs. Assuming the dc bus voltage is constant at

$$V_{BUS} = 230 \cdot \sqrt{2} \ V \tag{13}$$

the three-phase inverter losses are modeled as:

$$P_{INV} = 3 \cdot (\tfrac{1}{2} \cdot V_{BUS} \cdot I_M \cdot f_S \cdot \left(t_r + t_f \right) +$$
$$\tfrac{1}{2} \cdot V_{BUS} \cdot I_M \cdot f_S \cdot t_{rr} + I_M{}^2 \cdot R_{DS})$$
$$= 1.98 \cdot I_M + 3.57 \cdot I_M{}^2 \tag{14}$$

where I_M is the motor current, t_{rr} the reverse recovery time of the antiparallel diodes of the power MOSFET switching device, and R_{DS} is the ON resistance of the power devices.

The loss model of the front-end full-wave bridge rectifier circuit is:

$$P_{BR} = 2 \cdot V_D \cdot I_{IN} = 2 \cdot V_D \cdot \frac{P_{IN}}{V_{IN}}$$
$$= 2 \cdot 0.7 \cdot \frac{P_{IN}}{230} = 0.0061 \cdot P_{IN} \tag{15}$$

where V_D is the voltage drop across one of four bridge rectifier diodes, I_{IN} is the input current, and P_{IN} is the input power. The drive efficiency is derived from the inverter losses and the bridge rectifier losses. Based on these, the maximum inverter and bridge rectifier losses are estimated to be 40.8 and 6.21W, respectively, giving total losses of 47W.

Cooling Design

Based on the estimation of 47W losses, the compactness requirement in the drive packaging requires the smallest heatsink with forced-air cooling. A compact heatsink, which could satisfy all the requirements including the most crucial one of low-cost until a heatsink with dense small thin fins and allowing a turbulent air flow, is utilized in this design and layout to meet the compactness requirements.

PCB Layout Design and Final Assembly

Based on the heatsink dimension of 2.4 square inches and the final package volume requirement of 100 cubic inches, it became necessary to develop the layout of the power, controller, dc link filter, power supplies, fuses and connector around these specifications. The controller boards were split into two boards with dimensions of 2.45" × 5.1" and the power board connections were arranged in a printed circuit board (PCB) of 2.87 square inches. The drive circuit was divided into three double-sided PCBs, namely control board, driver board, and power board, as shown in Figure 13. The control board and driver board were implemented on the 5.0"× 2.4" PCBs. They contain the housekeeping power supply and the PI controller and the sine wave generator, and the PWM circuit and the gate drive IC, respectively. The power board (2.8"× 2.8") contains the bridge rectifier, the power devices, and the rest of the power circuit. The bridge rectifier and the power devices were mounted on the 2.4"× 2.4"× 0.5" heatsink, which also has a small fan attached to it. The three PCBs were assembled to form a 'Π' with the control board and the driver board at the sides, and the power board at the top, so as to enclose the dc bus electrolytic capacitors. A 6.0"× 4.3"× 2.9" enclosure was designed for the drive as follows: The top two pieces are folded to form two 'L's along the dotted line. When put together, they form a box whose front and back are the other two pieces. There is a hole in the middle of the front piece for mounting a potentiometer, if one is used to give the speed command.
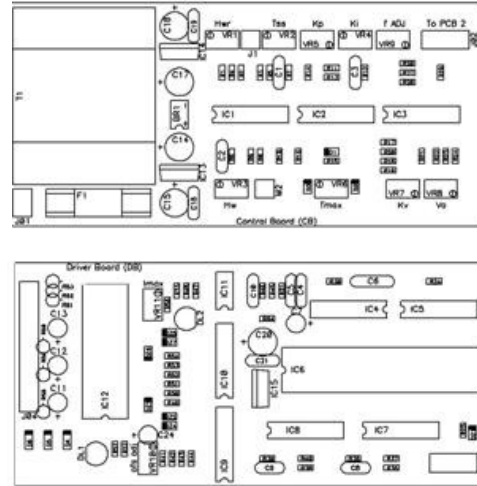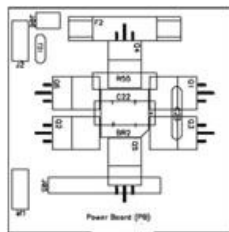

Figure 13. Proposed three PCBs to enclose all electronic circuitry (from top: power, driver, and control boards)
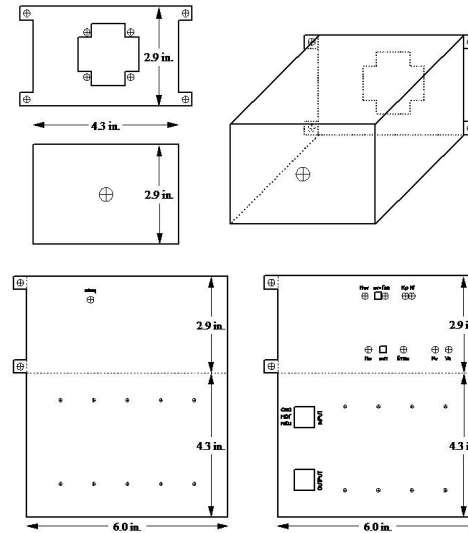

Figure 14. Proposed enclosure design

Figure 15. Comparison of the developed inverter (left) with a commercial one

The four holes at the edges of the rear piece were used for the mounting of the drive. The final enclosure assembly had the dimensions of 4.3"x 2.9"x 7" including heatsink and fan with an overall packaging volume of 87 cubic inches, thus

satisfying the packaging specification of less than 100 cubic inches. The proposed enclosure design is shown in Figure 14 and the prototype VSD is compared with Toshiba's VF-SX inverter in Figure 15. The size of Toshiba's inverter is 4.1"x 5.9"x 4.7" (approximately 114 cubic inches) with 1-hp output rating and contains many extra functions, which are not necessary for the low-cost fan/pump applications. The designed inverter is comparable to a commercial one in enclosure size.

Experimental Results

Experimental results on a 1-hp induction motor using the prototype VSD are presented in this section. The measured motor current waveform and its fast Fourier transform (FFT) results are shown in Figure 16. The FFT shows a strong fundamental frequency, 60Hz, component with negligible harmonics. The current ripple in the motor-current waveform can be reduced by increasing the frequency of the PWM. The overall efficiency of the motor drive is both calculated using procedures outlined in [11] and measured as shown in Figure 17 for a fan load. The efficiency of both methods shows a close match over the
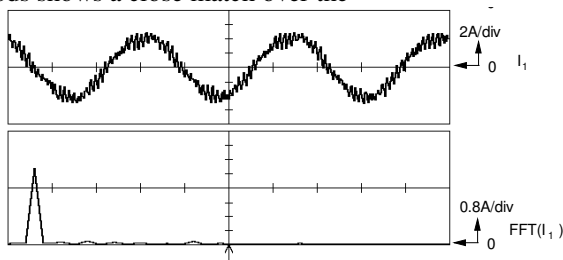
Figure 16. Motor current (Horizontal: 5 ms/div) and FFT (Horizontal: 100 Hz/div)
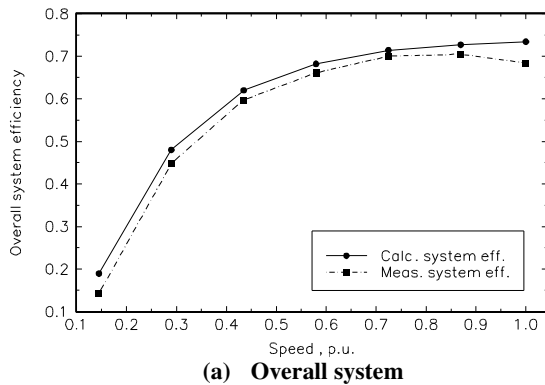
(a) Overall system
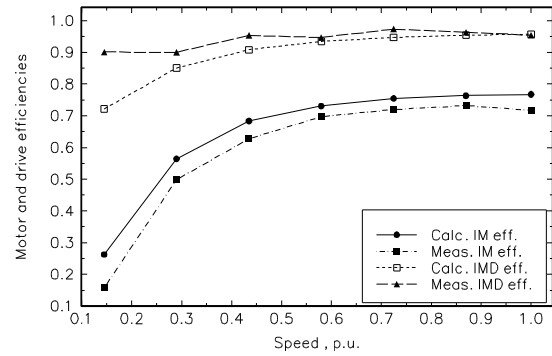
(b) Motor and inverter
Figure 17. Predicted and measured efficiencies

entire speed range. Figure 17(b) shows the predicted and measured induction motor and drive efficiencies that contributed to the system efficiency curves shown in Figure 17(a).

Topics for Electric-Motor Drives Courses

With the prototype IMD, the following topics are valuable for the electric motor drives course: principles and operations of the three-phase rectifier, SPWM, three-phase inverter, V/Hz control technique, three-phase sine wave generation, PI controller, gate drive circuit, soft-start circuit, torque-limiting circuit, VCO, and triangular waveform generation circuit. The layout design of the developed circuitry on PCB to optimize the power dissipation and EMI emission is very useful for the development of a VSD in the real world. Tuning and adjustment of the VSD provides plenty of hands-on experience to the students.

Conclusion

A high-density package of less than 100 cubic inches, 1-hp IMD with discrete analog and digital components have been designed, implemented and tested for emerging high-volume VSD applications. The design details and considerations of the controller, converters, their layouts and packaging, thermal design and overall packaging were systematically developed to assist in the development of other drives of various sizes. The overall VSD system efficiency and induction motor efficiency are obtained analytically and empirically. Both results were well matched with each other over the entire motor speed range. In conclusion, various teaching components are identified for electric motor drives courses.

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Biography

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