A Novel Five-Input Configurable Cell Based on Single Electron Transistor Minority Gates

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Abstract

Single Electron Technology (SET) is one of the future technologies that can be distinguished not only by its very small device size but also by its low power dissipation. The purpose of this paper is to introduce a five-input configurable SET cell based on single electron transistor minority gates. The proposed cell accepts five signals as its inputs and produces two complementary outputs. By applying appropriate input logic to the control gate(s), the cells can act as non-inverting/inverting buffers, Minority/Majority, two- and three-input NAND/AND or NOR/OR logic gates. As an application, a full adder, based on this proposed cell, was designed. All of the simulations for the proposed cell were done with SIMON 2.0.

Introduction

Current technologies like CMOS are predicted to encounter technological limitations [1], [2]. Further progress of such integration scale technology will be limited by a number of physical effects such as power dissipation [3]. Due to the problem of successfully scaling CMOS technology to meet the increased performance, density, and decreased power dissipation required for future technology generations, new technologies that will completely or partially replace silicon are being researched [3], [4]. Among the emerging technologies which strive to address these shortcomings is single electron technology (SET). SET uses a coulomb blocked effect and works by controlling the transfer of electrons one at a time [5], hence the device size and power dissipation decrease significantly [2], [5], [6]. These two properties, size and power, allow large density integration without exceeding the power density physical limits [7].

In this paper, a five-input single electron transistor-based configurable cell is introduced. With different configurations of these cells, functions such as non-inverting/ inverting buffers, Minority/Majority, two- and three-input NAND/AND or NOR/OR logic gates can be gained. As an application, a full adder is designed by using proposed cell.

The Proposed Design

The proposed cell accepts five input signals and produces two complementary outputs. As shown in Figure 1, each cell consists of two, five-input minority gates which are based on single electron transistors [8], which themselves are serially connected to each other. In the second Minority gate, if two of the five inputs are connected to a logical 1 and another two to a logical 0, the output of the gate will be a complement of the fifth input, which is connected to the output of the first minority gate. The Boolean function of output1 and output2 can be described by Equations (1) and (2), which are known as minority and majority functions, respectively.

$$OUTPUT1 = Minority(a,b,c,d,e) = \overline{a.b.c + a.b.d + a.b.e + a.c.d + a.c.e + a.d.e + b.c.d + b.c.e + b.d.e + c.d.e} \quad (1)$$

$$OUTPUT2 = Majority(a,b,c,d,e) = a.b.c + a.b.d + a.b.e + a.c.d + a.c.e + a.d.e + b.c.d + b.c.e + b.d.e + c.d.e \quad (2)$$

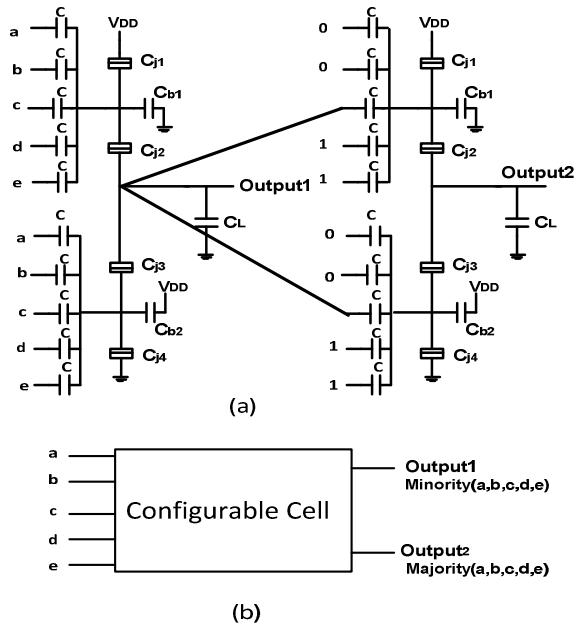

Figure 1. (a) Proposed Cell (b) The block diagram

In order to achieve a two-input NAND/AND gate or a two-input NOR/OR gate, two of the five inputs to the cell should be fixed to a logical 0 or 1 and another one to a logical 1 or 0, respectively. This can be illustrated by the following equations:

$$\text{OUTPUT1} = \text{Minority}(a,b,0,0,1) = \overline{a.b.0 + a.b.0 + a.b.1 + a.0.0 + a.0.1 + a.0.1 + b.0.0 + b.0.1 + b.0.1 + 0.0.1} = \overline{a.b} \equiv \text{NAND}(a,b) \quad (3)$$

$$\text{OUTPUT2} = \text{Majority}(a,b,0,0,1) = a.b.0 + a.b.0 + a.b.1 + a.0.0 + a.0.1 + a.0.1 + b.0.0 + b.0.1 + b.0.1 + 0.0.1 = a.b \equiv \text{AND}(a,b) \quad (4)$$

$$\text{OUTPUT1} = \text{Minority}(a,b,1,1,0) = \overline{a.b.1 + a.b.1 + a.b.0 + a.1.1 + a.1.0 + a.1.0 + b.1.1 + b.1.0 + b.1.0 + 1.1.0} = \overline{a+b} = \text{NOR}(a,b) \quad (5)$$

$$\text{OUTPUT2} = \text{Majority}(a,b,1,1,0) = a.b.1 + a.b.1 + a.b.0 + a.1.1 + a.1.0 + a.1.0 + b.1.1 + b.1.0 + b.1.0 + 1.1.0 = a+b = \text{OR}(a,b) \quad (6)$$

A three-input NAND/AND function can be represented by setting two inputs to a logical 0 (d=e=0) such that the Boolean function for output1 and ouput2 would be $\overline{abc}$ and abc, respectively. Similarly, to design a three-input NOR/OR gate, two inputs of a five-input minority gate should be set to a logical 1 (d=e=1), making the Boolean function for output1 equal to $\overline{a+b+c}$ and output2 equal to $a+b+c$.

If two of cell's inputs are a logical 1 and two are a logical 0, then the gate will act as an inverting/non-inverting buffer. To achieve a three-input minority/majority cell, one of the inputs should be set to a logical 1, and another one to a logical 0. This can be determined using Equations (7) and (8):

$$\text{OUTPUT1} = \text{Minority}(a,b,c,0,1) = \overline{a.b.c + a.b.0 + a.b.1 + a.c.0 + a.c.1 + a.0.1 + b.c.0 + b.c.1 + b.0.1 + c.0.1} = \text{Minority}(a,b,c) \quad (7)$$

$$\text{OUTPUT2} = \text{Majority}(a,b,c,0,1) = a.b.c + a.b.0 + a.b.1 + a.c.0 + a.c.1 + a.0.1 + b.c.0 + b.c.1 + b.0.1 + c.0.1 = \text{Majority}(a,b,c) \quad (8)$$

Using the SIMON simulator [9] with simulation parameters of $C_{j1}=C_{j4}=1aF$, $C_{j2}=C_{j3}=2aF$, $C_{b1} = C_{b2}=9aF$, $C_L=24aF$, $R_j=100\ k\Omega$, $C=0.6aF$, $V_{DD}=6.5mV$, logic 1=6.5mV, and logic 0=0V, the correct operation of the proposed cell is illustrated as shown in Figures 2-5.

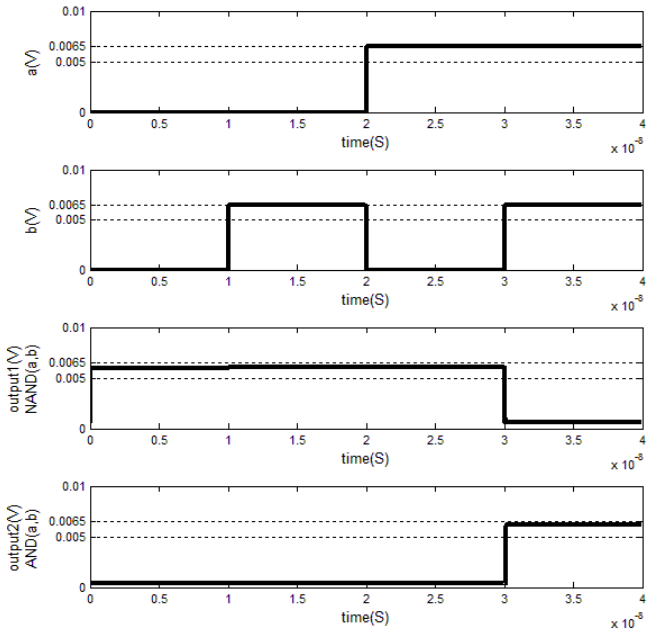

Figure 2. The Cell Output Waveforms for the Two-Input NAND/AND (c =d=0, e=1)

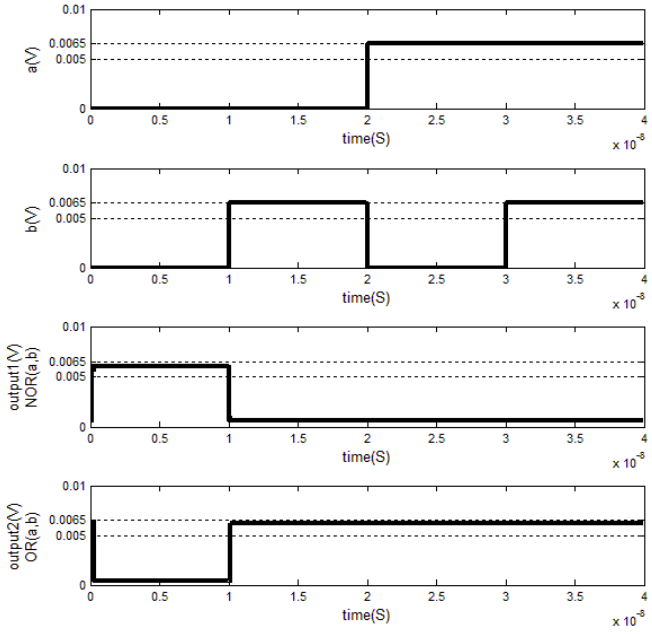

Figure 3. The Cell Output Waveforms for the Two-Input NOR/OR(c=d=1, e=0)

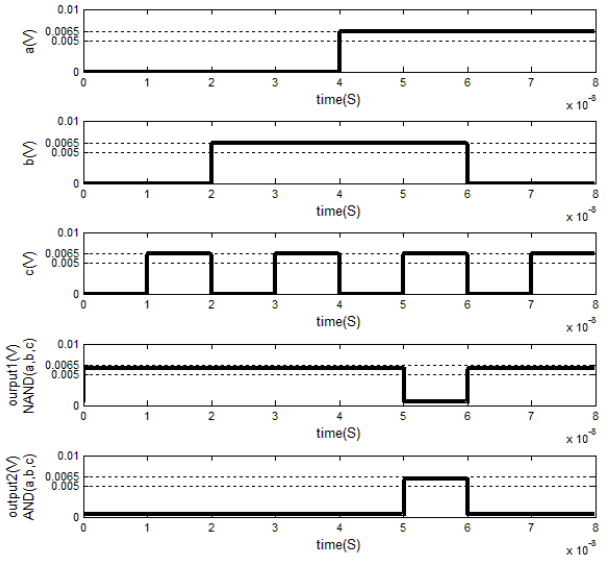

Figure 4. The Cell Output Waveforms for the Three-Input NAND/AND (d=e=0)

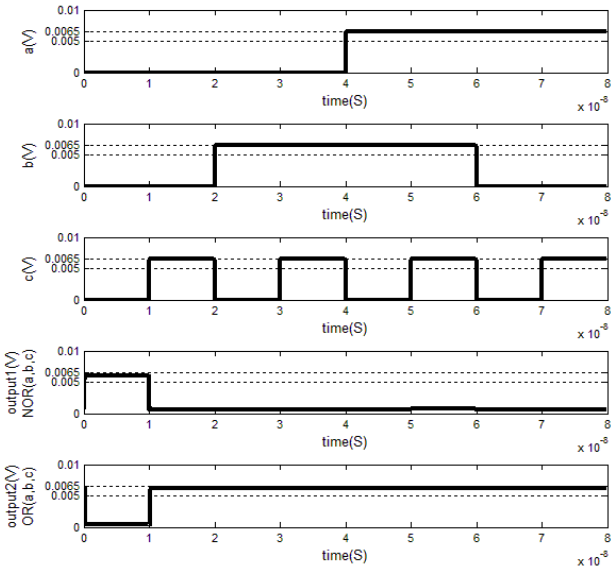

Figure 5. The Cell Output Waveforms for the Three-Input NOR/OR(d=e=1)

Designing a Full Adder using the Proposed Cell

Full adders are one the most important parts of each an arithmetic logic unit (ALU). Any kind of improvements in full-adder design result in significant improvement in ALU functionality. Hence, different devices are used in order to implement full adders [3], [10]. The functionality of a 1-bit full adder with a, b, and c_{in} (Input Carry) inputs, and sum and c_{out} (Output Carry) outputs, can be described by the following equations [11]:

$$c_{out} = ab + ac_{in} + bc_{in} = \text{Majority}(a, b, c_{in}) \quad (9)$$

$$\text{Sum} = (a + b + c_{in}) + a.b.c_{in} = \text{Majority}(a, b, c_{in}, \overline{c_{out}}, \overline{c_{out}}) \quad (10)$$

The basic idea of the design proposed in this study is that the c_{out} function would be the same as the three-input majority function. Also, the sum output can be generated from $\overline{c_{out}}$ by using a five-input majority function with a, b, c_{in}, and two $\overline{c_{out}}$ inputs, as shown in Table 1. With regard to Equations (9) and (10), the block diagram and simulation results of a full adder using this proposed cell is depicted in Figure (6).

Table 1. Functionality of 1-bit Full-Adder

a	b	c_{in}	$\overline{c_{out}}$	$\text{Majority}(a, b, c_{in}, \overline{c_{out}}, \overline{c_{out}})$	Sum
0	0	0	1	0	0
0	0	1	1	1	1
0	1	0	1	1	1
0	1	1	0	0	0
1	0	0	1	1	1
1	0	1	0	0	0
1	1	0	0	0	0
1	1	1	0	1	1

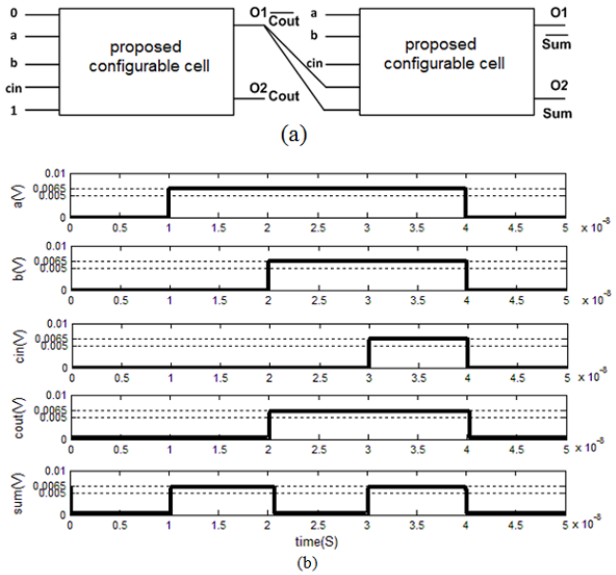

Figure 6. (a) Block Diagram of Full Adder Based on Proposed Cell (b) Input and Output Waveforms for the Proposed Full Adder

Conclusion

In this study, a five-input configurable cell based on single electron technology was introduced which is suitable for implementing inverting/non-inverting buffer, Minority/ Majority, NAND/AND and NOR/OR majority logic gates. As an application, a full adder based on a five-input cell was presented. All of the simulations were performed using a SIMON simulator.

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Biographies

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